

## CLAIMS

What is claimed is:

1 A method for processing cache memory accesses in a computing  
 2 system having a requester to submit memory access addresses for requested  
 3 data, and having a tag memory to store tag addresses corresponding to  
 4 addresses stored in the cache memory, the method comprising:  
 5 retrieving a stored tag address from the tag memory in response to  
 6 the requester submitting a memory access address;  
 7 performing a first comparison of the memory access address to the  
 8 stored tag address to determine whether the requested data is stored in the cache  
 9 memory;  
 10 monitoring for errors in the stored tag address, wherein the  
 11 monitoring is performed contemporaneously with the first comparison of the  
 12 memory access address and the stored tag address;  
 13 if a tag address error is detected, disregarding the first comparison,  
 14 correcting the tag address error, and performing a second comparison of the  
 15 memory access address and the corrected tag address to determine whether the  
 16 requested data is stored in the cache memory; and  
 17 if no tag address error is detected, utilizing results of the first  
 18 comparison to determine whether the requested data is stored in the cache  
 19 memory.

1 2. The method of Claim 1, wherein monitoring for errors comprises  
 2 storing a single error correction code with the data stored in the tag memory.

1           4. ~~The method of Claim 1, wherein the first comparison compares only~~  
2     ~~the stored tag address with the memory access address, and disregards~~  
3     ~~comparison of any stored error correction code bits.~~

1           6.       The method of Claim 1, wherein performing the first comparison and  
2       monitoring for errors in the stored tag address occur contemporaneously with  
3       correcting the tag address error and performing the second comparison.

1           7.       The method of Claim 1, wherein correcting the tag address error and  
2       performing the second comparison are initiated upon recognition of a tag address  
3       error.

1           8.     The method of Claim 1, wherein disregarding the first comparison  
2     comprises blocking passage of the results of the first comparison through an  
3     output gate.

1           9.   The method of Claim 8, wherein blocking passage of the first  
2   comparison results comprises:  
3               providing an error signal to the output gate when a tag address error  
4   is detected; and

5            disabling an output of the output gate upon receipt of the error  
6    signal.

1            10.    The method of Claim 9, further comprising enabling the tag address  
2    error to be corrected and the second comparison of the memory access and  
3    corrected tag addresses to be performed in response to the error signal.

1            11.    A cache hit detector, comprising:

2            (a)    a tag memory to store tag addresses corresponding to addresses  
3    currently cached;

4            (b)    a fast hit detection circuit, comprising:

5                    (i)    a first address compare module coupled to the tag memory to  
6    receive a tag address and to compare the tag address to a requested  
7    address;

8                    (ii)   an error detector coupled to the tag memory to receive the  
9    tag address and to determine whether there are any errors in the tag  
10   address;

11                  (iii)   a gated output module coupled to the first address compare  
12   module and the error detector to output a fast hit indication if and only if no  
13   error is discovered by the error detector and the requested address is  
14   stored in the tag memory;

15            (c)    a slow hit detection circuit, comprising:

16                    (i)    an error correction circuit coupled to the tag memory to  
17   receive the tag address and to correct errors in the tag address; and

18                    (ii)   a second address compare module coupled to the error  
19   correction circuit to receive the corrected tag address and to compare the  
20   corrected tag address to a current address.

1           12. The cache hit detector as in Claim 11, wherein the fast hit detection  
2 circuit and the slow hit detection circuit are coupled in parallel such that the first  
3 address compare module and the error detector perform operations concurrently  
4 with operations of the second address compare module and the error correction  
5 circuit.

1           13. The cache hit detector as in Claim 11, further comprising latching  
2 means to coordinate timing between the fast hit detection circuit and the slow hit  
3 detection circuit.

1           14. The cache hit detector as in Claim 11, wherein the tag memory  
2 further stores an error correction code for each block of data stored in the tag  
3 memory, wherein each block of data is associated with a single error correction  
4 code, and the single error correction code provides error correction capabilities  
5 for the stored tag address and a plurality of configuration fields.

1           15. The cache hit detector as in Claim 11, wherein the first address  
2 compare module and the error detector are coupled in parallel to  
3 contemporaneously compare the tag address to a requested address and  
4 determine whether there are any errors in the tag address.

1           16. The cache hit detector as in Claim 11, further comprising:  
2           a first latch coupled to the first address compare module to latch  
3 comparison results;  
4           a second latch coupled to the error detector to latch a resulting error  
5 indicator signal; and  
6           wherein the comparison results and the error indicator signal are not  
7 passed to the gated output until both the comparison results and the error  
8 indicator signal are available at the first and second latches, and until

9 simultaneously clocked to concurrently provide the comparison results and the  
10 error indicator signal to the gated output.

1 17. The cache hit detector as in Claim 11, wherein the error detector  
2 determines whether there are any single bit errors in the tag address.

1 18. A data processing system comprising:

2 (a) a main memory module for storing data;

3 (b) at least one cache memory coupled to the main memory module to  
4 cache at least a portion of the data stored in the main memory module;

5 (c) at least one processing unit to process data and to control data access  
6 with the main memory module and the cache memory, the processing unit  
7 comprising:

8 (1) a tag memory to store tag addresses corresponding to  
9 addresses currently cached;

10 (2) a fast hit detection circuit, comprising:

11 (i) a first address compare module coupled to the tag  
12 memory to receive a tag address and to compare the tag address to  
13 a requested address;

14 (ii) an error detector coupled to the tag memory to receive  
15 the tag address and to determine whether there are any errors in the  
16 tag address;

17 (iii) a gated output module coupled to the first address  
18 compare module and the error detector to output a fast hit indication  
19 if and only if no error is discovered by the error detector and the  
20 requested address is stored in the tag memory;

21 (3) a slow hit detection circuit, comprising:

22 (i) an error correction circuit coupled to the tag memory to  
23 receive the tag address and to correct errors in the tag address; and

1           19. The data processing system of Claim 18, wherein the fast hit  
2 detection circuit and the slow hit detection circuit are configured in parallel such  
3 that the first address compare module and the error detector perform operations  
4 concurrently with operations of the second address compare module and the error  
5 correction circuit.

1            21.    A cache hit detector, comprising:

2            (a)    means for storing tag memory addresses corresponding to

3 addresses of data currently stored in cache memory;

4            (b)    means for providing alternate cache hit detection via concurrent

5 processing on each of at least two cache hit detection paths, the alternate cache

6 hit detection means comprising:

7            (1)    first hit detection path means for detecting cache hits without

8 first performing error detection and correction;

9            (2)    second hit detection path means for detecting cache hits, the

10 second hit detection path means comprising:

11            (i)    means for detecting errors in the tag memory address;

12            (ii)   means for correcting the tag memory address if errors

13 in the tag memory address are discovered;

- 14 (iii) means for detecting for cache hits using the corrected  
15 tag memory address if errors in the tag memory address are  
16 discovered; and  
17 (iv) means for disabling the first hit detection path means if  
18 errors in the tag memory address are discovered.

- 1  
2 22. The cache hit detector as in Claim 21, further comprising means for  
3 coordinating timing between the first hit detection path means and the second hit  
detection path means.

002075-52920260